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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/834696	
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	First Named Inventor	King, Jerrold	
	Art Unit	2827	
	Examiner Name	James M. Mitchell	
Total Number of Pages in This Submission	25	Attorney Docket Number	MICR135.02

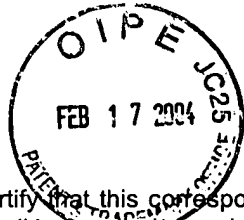
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Date	February 12, 2004

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**IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE**

INVENTOR: Jerrold King et al.

SERIAL NO.: 09/834,696

GROUP ART UNIT: 2822

FILED: April 12, 2001

EXAMINER: J. Mitchell

TITLE: Semiconductor Chip Package

APPELLANTS'/APPLICANTS' OPENING BRIEF ON APPEAL

1. REAL PARTY IN INTEREST.

Micron Technology, Inc. owns this patent application.

2. RELATED APPEALS AND INTERFERENCES.

There are no other appeals or interferences known to Appellants, Appellants' legal representative or the Assignee which will affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

3. STATUS OF CLAIMS.

Claims 19, 23 and 24 are pending. Claims 1-18 (from the parent case) and Claims 20-22 have been canceled. All pending claims, Claims 19, 23 and 24 are appealed.

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4. STATUS OF AMENDMENTS.

The Response filed October 14, 2003 sought entry of an amendment amending Claim 24 and canceling Claims 19 and 23, in an effort to place the case in condition for allowance. The Examiner declined to enter the amendment. The proposed amendment to Claim 24 is discussed below in the Argument section with regard to Issue No. 2.

5. SUMMARY OF INVENTION.

The claims are directed to a semiconductor chip package in which the external electrodes are not connected directly to bond pads or electrical traces on the semiconductor chip. Hence, the size of the package and the configuration of the electrode array can remain the same even as the chip is made smaller, thus allowing the package to be constructed to a standard format. Specification, page 4, lines 20-25. For example, the semiconductor chip package recited in Claim 19 includes conductive leads electrically connected to and extending over a surface of the chip (e.g., leads 12 in Figs. 1-4), a continuous body of encapsulating material covering at least a portion of the chip (e.g., encapsulating material 26 in Figs. 1-4), and electrodes each having a first portion disposed in the encapsulating material and contacting a conductive lead and a second portion protruding from the encapsulating material (e.g., external electrodes 28 in Figs. 1-4). The body of encapsulating material fully encapsulates the conductive leads except for the point of contact with the electrodes where the encapsulating material is necessarily displaced to allow the electrode to contact the lead.

6. ISSUES.

1. Do electrodes 8 or bumps 10 in Ichiyama (5,373,190) **extend** over semiconductor element 1 as recited in Claims 19, 23 and 24?
2. Does Ichiyama teach or suggest the combination of three conductive paths in the structural configuration recited in Claim 24?

7. GROUPING OF CLAIMS.

Applicant proposes the following grouping of claims according to the Issues noted above in Section 6.

Issue No. 1: Claims 19, 23 and 24. Claims 19 and 23 stand or fall together. Claim 24 stands but does not fall with Claims 19 and 23.

Issue No. 2: Claim 24.

8. ARGUMENT.

ISSUE NO. 1

Electrodes 8 And Bumps 10 In Ichiyama Do Not Extend Over The Semiconductor Chip As Required To Support The Rejection Of Claims 19, 23 And 24

Claim 19 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Ichiyama (U.S. Patent No. 5,373,190). A claim is anticipated only if each and every element in the claim is found expressly or inherently in the reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989).

Claim 19 requires conductive leads electrically connected to and extending over a surface of the chip. In support of the rejection, the Examiner asserts that electrodes 8 or bumps 10 in Ichiyama are the conductive leads recited in Claim 19.

Extend means "1. to stretch or draw out to full length.... 2. to stretch or draw outward. ... 4. to make longer, as to reach a particular point...." Random House Webster's College Dictionary (2000). Electrodes 8 and bumps 10 in Ichiyama do not extend over semiconductor element 1 as required in Claim 19. As shown in Figs. 6 and 7 of Ichiyama, electrodes 8 and bumps 10 both have a circular footprint -- they are dots over semiconductor element 1. They are not the least bit elongated and, therefore, cannot and do not extend anywhere over semiconductor element 1.

This distinction is significant for the reasons noted in the Background section of the present application. Ichiyama's semiconductor package is like the chip scale packages discussed in the Background section of the Specification at page 2, lines 29-34, except that Ichiyama uses a hard conductor terminal instead of solder balls. One disadvantage of this design, in which a non-elongated/one-dimensional external

contact is positioned directly over the electrical contact on the surface chip, is that the external contacts and the corresponding contacts on a printed circuit board must be reconfigured each time the chip is made smaller. Specification, page 3, lines 5-11. This is one of the problems addressed by the claimed invention, in which the external contacts are indirectly connected to the chip through elongated leads that extend over the surface of the chip -- the external contacts and the corresponding contacts on a printed circuit board need not be reconfigured when the chip is made smaller.

The Examiner asserts in reply to Applicants' position that:

"Because the limitations argued by applicant are not in claim 19, the argument is deemed moot. The ordinary plain meaning of a lead extending over a chip, which is recited in the claim, encompasses in scope, merely a lead spread over certain distance that covers a portion of the chip; Ichiyama clearly shows those features." Office Action mailed 8/13/03, paragraph 11.

The Examiner's assertion is not correct. The ordinary plain meaning of the term "extending" as reflected in Webster's Collegiate Dictionary noted above requires some type of elongation or stretching out. In the context of Claim 19, this elongation or stretching out must be over the semiconductor chip. In a dimension along the surface of semiconductor element 1 in Ichiyama, electrodes 8 and bumps 10 both have a one-dimensional/circular footprint -- they are dots over the surface of semiconductor element 1. A dot cannot reasonably be deemed to be elongated or stretched out over anything. If, as the Examiner asserts, any structure positioned "over" the semiconductor chip is deemed to be "extending over" the semiconductor chip, then he has effectively read "extending" out of the claim. A lead "over" a chip is not necessarily a lead "extending over" a chip. Neither electrodes 8 nor bumps 10 in Ichiyama extend over the surface of the semiconductor chip as required in Claim 19.

Claims 23 and 24 stand rejected under 35 U.S.C. § 103 as being obvious over Ichiyama in combination with Ehata (JP59148352). Claims 23 and 24, like Claim 19, require conductive leads electrically connected to and extending over the chip. For the reasons noted above for Claim 19, Ichiyama also does not teach or suggest this element of Claims 23 and 24.

ISSUE NO. 2

Ichiyama Does Not Teach Or Suggest The Combination Of Three Conductive Paths In The Structural Configuration Recited In Claim 24

Claim 24 recites a package that includes three so-called (by the Examiner) "conductive paths" -- (1) bond pads along a surface of the chip, (2) conductive leads attached to insulating material on the surface of the chip and electrically connected to the bond pads, and (3) solder balls contacting the conductive leads. Holes in the insulating material enable the electrical connection to the bond pads. A continuous body of encapsulating material covers at least a portion of the chip and the conductive leads.

Claim 24 stands rejected under 35 U.S.C. § 103 as being obvious over Ichiyama in combination with Ehata (JP59148352). The Examiner relies on Ichiyama to show all elements of Claim 24 except the solder ball. Ehata is cited to show a solder ball.

The Examiner has not specifically addressed the insulating material limitation recited in Claim 24. Ichiyama teaches only a continuous body of encapsulating material. Ichiyama does not teach or suggest insulating material on the surface of the chip and a body of encapsulating material. In his discussion of Ichiyama in paragraph 4 of the Office Action mailed 8/13/03, the Examiner refers to "a continuous body of insulating encapsulating material (4, via epoxy)" and in paragraph 8 to "the insulating material." Nowhere does the Examiner specifically assert that Ichiyama teaches both insulating material on the surface of the chip and a continuous body of encapsulating material. These are discrete elements in Claim 24 and the Examiner carries the burden of showing that both elements are taught or suggested in the art. Absent such a showing, the Examiner has failed to establish a prima facie case of obviousness and the Section 103 rejection should be withdrawn.

Applicants sought to amend Claim 24 in response to the final action to correct an obvious error that had gone undetected until then -- each lead is connected to a bond pad and extends over the surface of the chip, not over the bond pads. (None of the embodiments shown in the drawings include leads extending over the bond pads.) Applicants also sought to amend Claim 24 to make it more clear that the insulating material and encapsulating material are discrete elements, to avoid any suggestion that the encapsulating material in Ichiyama might somehow be deemed to satisfy both claim elements. The proposed amended Claim 24 is set forth below.

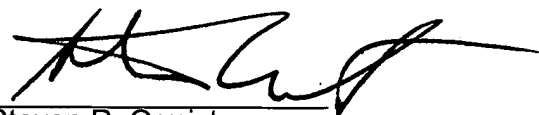
24.(proposed amendment) A semiconductor chip package, comprising:
a semiconductor chip having bond pads aligned along a surface of the chip;
insulating material on the surface of the chip, the insulating material having
holes therein to enable electrical connection to the bond pads;
conductive leads attached to the insulating material, each lead electrically
connected to a bond pad and extending over the surface of the chip ~~bond pads~~;
a continuous body of encapsulating material, discrete from the insulating
material, covering at least a portion of the chip and at least a portion of the
conductive leads; and
solder balls each having a first portion disposed in the encapsulating material
and contacting a conductive lead and a second portion protruding from the
encapsulating material.

The Examiner declined to enter the amendment to Claim 24 on the grounds
that the amendments (1) "raise new issues and would require further consideration
and/or search" and (2) "on cursory consideration the request does not appear to
overcome the rejections."

Applicants request that the Board enter the amendments to Claim 24. The
first part of the amendment, reciting conductive leads "extending over the surface of
the chip ~~bond pads~~", corrects an obvious mistake and does not raise any new issues
-- this is the configuration for the conductive leads recited in Claims 19 and 23. The
second part of the amendment, reciting "a continuous body of encapsulating
material, discrete from the insulating material", makes more clear a structural
limitation already in the claim as originally presented. This second part of the
amendment also would not seem to raise any new issues.

Respectfully submitted,
Jerrold King et al.

By



Steven R. Ormiston
Reg. No. 35,974
(208) 433-1991

APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

19. A semiconductor chip package, comprising:
a semiconductor chip;
conductive leads electrically connected to and extending over a surface of the chip;
a continuous body of encapsulating material covering at least a portion of the chip;
electrodes each having a first portion disposed in the encapsulating material and contacting a conductive lead and a second portion protruding from the encapsulating material; and
the body of encapsulating material fully encapsulating the conductive leads except for the point of contact with the electrodes where the encapsulating material is necessarily displaced to allow the electrode to contact the lead.

23. A semiconductor chip package, comprising:
a semiconductor chip;
conductive leads electrically connected to and extending over a surface of the chip;
a continuous body of encapsulating material covering at least a portion of the chip and at least a portion of the conductive leads; and
solder balls each having a first portion disposed in the encapsulating material and contacting a conductive lead and a second portion protruding from the encapsulating material.

24. A semiconductor chip package, comprising:
a semiconductor chip having bond pads aligned along a surface of the chip;
insulating material on the surface of the chip, the insulating material having holes therein to enable electrical connection to the bond pads;
conductive leads attached to the insulating material, each lead electrically connected to and extending over the bond pads;
a continuous body of encapsulating material covering at least a portion of the chip and at least a portion of the conductive leads; and

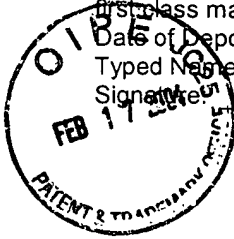
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Date of Deposit: February 12, 2004

Typed Name of Person Mailing Paper or Fee: Tanra F. Paulin

Signature: 



**IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE**

INVENTOR: Jerrold King et al.

SERIAL NO.: 09/834,696

GROUP ART UNIT: 2822

FILED: April 12, 2001

EXAMINER: J. Mitchell

TITLE: Semiconductor Chip Package

APPELLANTS'/APPLICANTS' OPENING BRIEF ON APPEAL

1. REAL PARTY IN INTEREST.

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2. RELATED APPEALS AND INTERFERENCES.

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5. SUMMARY OF INVENTION.

The claims are directed to a semiconductor chip package in which the external electrodes are not connected directly to bond pads or electrical traces on the semiconductor chip. Hence, the size of the package and the configuration of the electrode array can remain the same even as the chip is made smaller, thus allowing the package to be constructed to a standard format. Specification, page 4, lines 20-25. For example, the semiconductor chip package recited in Claim 19 includes conductive leads electrically connected to and extending over a surface of the chip (e.g., leads 12 in Figs. 1-4), a continuous body of encapsulating material covering at least a portion of the chip (e.g., encapsulating material 26 in Figs. 1-4), and electrodes each having a first portion disposed in the encapsulating material and contacting a conductive lead and a second portion protruding from the encapsulating material (e.g., external electrodes 28 in Figs. 1-4). The body of encapsulating material fully encapsulates the conductive leads except for the point of contact with the electrodes where the encapsulating material is necessarily displaced to allow the electrode to contact the lead.

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ISSUE NO. 1

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Ichiyama Does Not Teach Or Suggest The Combination Of Three Conductive Paths In The Structural Configuration Recited In Claim 24

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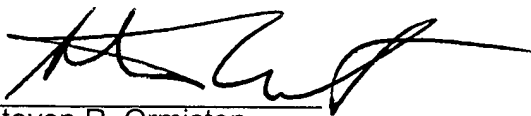
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holes therein to enable electrical connection to the bond pads;
conductive leads attached to the insulating material, each lead electrically
connected to a bond pad and extending over the surface of the chip ~~bond pads~~;
a continuous body of encapsulating material, discrete from the insulating
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and contacting a conductive lead and a second portion protruding from the
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amendment also would not seem to raise any new issues.

Respectfully submitted,
Jerrold King et al.

By


Steven R. Ormiston
Reg. No. 35,974
(208) 433-1991

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a semiconductor chip;
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a continuous body of encapsulating material covering at least a portion of the chip;
electrodes each having a first portion disposed in the encapsulating material and contacting a conductive lead and a second portion protruding from the encapsulating material; and
the body of encapsulating material fully encapsulating the conductive leads except for the point of contact with the electrodes where the encapsulating material is necessarily displaced to allow the electrode to contact the lead.

23. A semiconductor chip package, comprising:
a semiconductor chip;
conductive leads electrically connected to and extending over a surface of the chip;
a continuous body of encapsulating material covering at least a portion of the chip and at least a portion of the conductive leads; and
solder balls each having a first portion disposed in the encapsulating material and contacting a conductive lead and a second portion protruding from the encapsulating material.

24. A semiconductor chip package, comprising:
a semiconductor chip having bond pads aligned along a surface of the chip;
insulating material on the surface of the chip, the insulating material having holes therein to enable electrical connection to the bond pads;
conductive leads attached to the insulating material, each lead electrically connected to and extending over the bond pads;
a continuous body of encapsulating material covering at least a portion of the chip and at least a portion of the conductive leads; and

solder balls each having a first portion disposed in the encapsulating material and contacting a conductive lead and a second portion protruding from the encapsulating material.